AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method comprising:

configuring processors with multiple threads of execution to execute a critical section of code, the processors operable to execute the critical section in turns, each processor completing execution of the critical section during their respective turn, the processors comprising a functional pipeline in a network processor; and

controlling the threads of execution of the processors to avoid occurrence of idle time between execution of the critical section by the processors by executing threads within a processor in a sequential order,

wherein the processors are operable to execute at least two of the critical sections of code and one of the critical sections of code comprises a metering microblock and the another of the critical sections of code comprises a congestion avoidance microblock.

2. (Previously Presented) The method of claim 1 wherein controlling comprises:

enabling the threads of execution on each of the processors to execute in the sequential order via inter-thread signaling.

3. (Original) The method of claim 2 wherein enabling comprises:

enabling each thread, when such thread is executing, to execute a first instruction to cause an inter-thread signal to a next thread to be generated; and

enabling the thread to execute a second instruction, which causes the thread to wait for an inter-thread signal from a previous thread, only after a write latency required by the first instruction.

4. (Original) The method of claim 3 wherein the write latency comprises at least three instruction cycles.

5. (Original) The method of claim 3 wherein the processors each comprise a register through which an inter-thread signal to the next thread is given.

6. (Original) The method of claim 5 wherein the processors each comprise registers through which inter-thread, inter-processor signaling can occur.

7. (Original) The method of claim 6 wherein the processors use external registers to enable inter-thread, inter-processor signaling to occur.

8. (Original) The method of claim 2 wherein controlling further comprises:

enabling each thread of execution on each of the processors to relinquish control of a program comprising the critical section as soon as the critical section has been executed.

9. (Original) The method of claim 1 wherein controlling comprises:

enabling each thread of execution on each of the processors to relinquish control of the program comprising the critical section as soon as the critical section has been executed.

Claims 10 to 12 (Cancelled)

13. (Original) The method of claim 1 wherein the processors comprise a functional pipeline, and one or more of the critical sections of code are executed in the functional pipeline.

14. (Original) The method of 13 wherein one of the one or more critical sections of code comprises an Asynchronous Transfer Mode (ATM) receive processing microblock.

15. (Original) The method of claim 13 wherein one of the one or more critical sections comprises an ATM traffic management processing microblock.

16. (Currently Amended) A article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

configuring processors with multiple threads of execution to execute a critical section of code, the processors operable to execute the critical section in turns, each processor completing execution of the critical section during their respective turn, the processors comprising a functional pipeline in a network processor; and

controlling the threads of execution of the processors to avoid occurrence of idle time between execution of the critical section by the processors by executing threads within a processor in a sequential order,

wherein the processors are operable to execute at least two of the critical sections of code and one of the critical sections of code comprises a metering microblock and the another of the critical sections of code comprises a congestion avoidance microblock.

17. (Previously Presented) The article of claim 16 wherein controlling comprises:

enabling the threads of execution on each of the processors to execute in the sequential order via inter-thread signaling.

18. (Original) The article of claim 17 wherein enabling comprises:

enabling each thread, when such thread is executing, to execute a first instruction to cause an inter-thread signal to a next thread to be generated; and

enabling the thread to execute a second instruction, which causes the thread to wait for an inter-thread signal from a previous thread, only after a write latency required by the first instruction.

19. (Original) The article of claim 16 wherein controlling comprises:

enabling each thread of execution on each of the processors to relinquish control of the program comprising the critical section as soon as the critical section has been executed.

20. (Currently Amended) A network processor comprising:

a processor; and

multi-threaded processors, having threads of execution, configurable by the processor to execute a critical section of code and operable to execute the critical section in turns, each processor completing execution of the critical section during their respective turn, the multi-threaded processors comprising a functional pipeline in the network processor; and

wherein the threads of execution of the multi-threaded processors are controllable to avoid occurrence of idle time between execution of the critical section by the multi-threaded processors by executing threads within a processor in a sequential order,

wherein the multi-threaded processors are operable to execute at least two of the critical sections of code and one of the critical sections of code comprises a metering microblock and the another of the critical sections of code comprises a congestion avoidance microblock.

21. (Original) The network processor of claim 20 wherein each thread, when such thread is executing, is controllable to execute a first instruction to cause an inter-thread signal to a next thread to be generated, and the thread is further controllable to execute a second instruction, which causes the thread to wait for an inter-thread signal from a previous thread, only after a write latency required by the first instruction.

22. (Original) A network processor of claim 20 wherein each thread of execution on each of the multi-threaded processors is controllable to relinquish control of the program comprising the critical section as soon as the critical section has been executed.

23. (Currently Amended) A system comprising:

a memory system to store a critical section of code;

processors, coupled to the memory system, having multiple threads of execution to execute the critical section of code, the processors operable to execute the critical section in turns, each processor completing execution of the critical section during their respective turn, the processors comprising a functional pipeline in a network processor; and

wherein the threads of execution of the processors are controllable to avoid occurrence of idle time between execution of the critical section by the processors by executing threads within a processor in a sequential order,

wherein the processors are operable to execute at least two of the critical sections of code and one of the critical sections of code comprises a metering microblock and the another of the critical sections of code comprises a congestion avoidance microblock.

24. (Original) The system of claim 23 wherein each thread, when such thread is executing, is controllable to execute a first instruction to cause an inter-thread signal to a next thread to be generated, and the thread is further controllable to execute a second instruction, which causes the thread to wait for an inter-thread signal from a previous thread, only after a write latency required by the first instruction.

25. (Original) The system of claim 23 wherein each thread of execution on each of the multi-threaded processors is controllable to relinquish control of the program comprising the critical section as soon as the critical section has been executed.